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02/13/2004

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(Date)	ch 24, 2004	Mas	

APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO. 10/664,262 09/17/2003 Yong Meng Lee CS01-211

TITLE OF INVENTION: METHOD OF FORMING DOUBLE-GATED SILICON-ON-INSULATOR (SOI) TRANSISTORS WITH REDUCED GATE TO SOURCE-DRAIN OVERLAP CAPACITANCE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	05/13/2004
EXAMINER		ART UNIT	CLASS-SUBCLASS	]	
ISAAC, ST	ANETTA D	2812	438-151000	<b>-</b>	

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Please check the appropriate assignee category or categories (will not be printed on the patent);

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